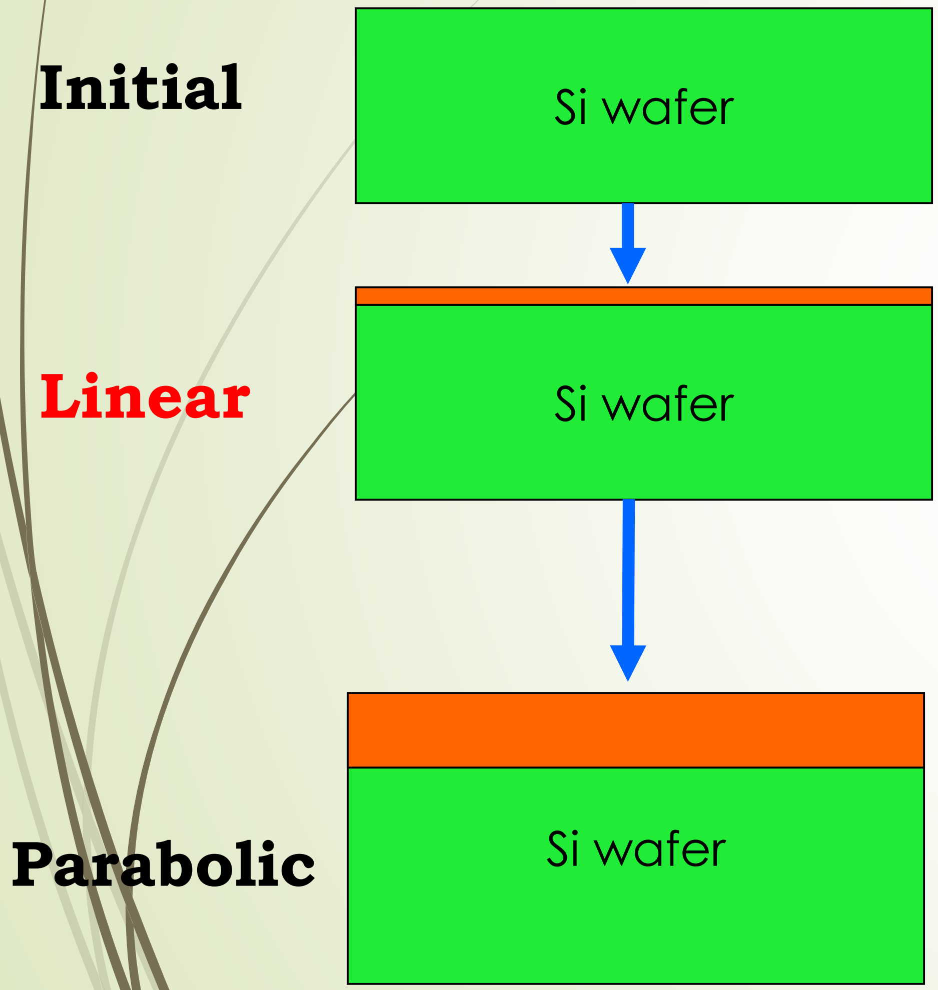
Lecture (2)

Thermal Oxidation of Silicon (Cont.)

SiO_2 Growth Stages



- In a furnace with O_2 gas environment
- Oxygen atoms combine readily with Si atoms
- **Linear- oxide** grows in equal amounts for each time $X_o(t) = \left(\frac{B}{A}\right)(t+\tau)$
- Around 500Å thick
- Above 500Å, in order for oxide layer to keep growing, oxygen and Si atoms must be in contact $X_o(t) = \sqrt{Bt}$

Factors Influencing Oxidation Rate

- **Oxidation rate is Controlled by:**

1. **Temperature**
2. **Wafer orientation**
3. **Pressure**
4. **Wafer dopant distribution**
5. **Impurities**
6. **Oxidation of polysilicon layers**

Factors Influencing Oxidation Rate

1. Temperature

A mathematical model for The temperature dependence of the oxidation growth rate is

$$D = D_o \, exp\,(-E_A/kT) \qquad (12)$$

where

D is the diffusion coefficient , $\boldsymbol{E_A}$ is the activation energy

T is the absolute temperature, **K** is Boltzmann constant=1.38x10^{23}

TABLE 3.1 Values for Coefficient D_0 and Activation Energy E_A for Wet and Dry Oxygen*

	Wet $O_2(X_i = 0$ nm)		Dry $O_2(X_i = 25$ nm)	
	D_0	E_A	D_0	E_A
<100> Silicon				
Linear (B/A)	9.70×10^7 μm/hr	2.05 eV	3.71×10^6μm/hr	2.00 eV
Parabolic (B)	386μm^{2}}/hr	0.78 eV	772μm^2/hr	1.23 eV
<111> Silicon				
Linear (B/A)	1.63×10^8μm/hr	2.05 eV	6.23μ10^{6}μm/hr	2.00 eV
Parabolic (B)	386μm^2/hr	0.78 eV	772μm^2/hr	1.23 eV

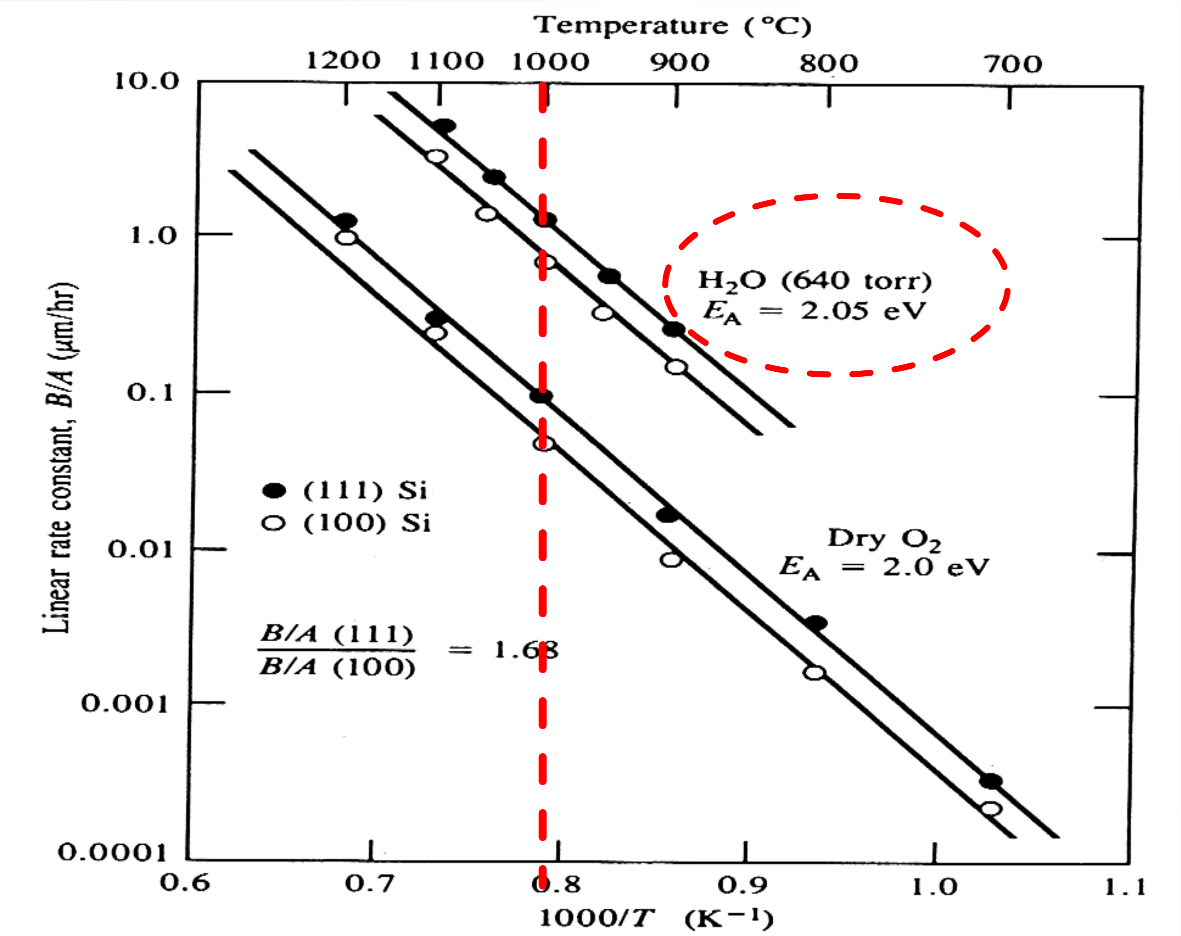
*Data from Ref.[9]

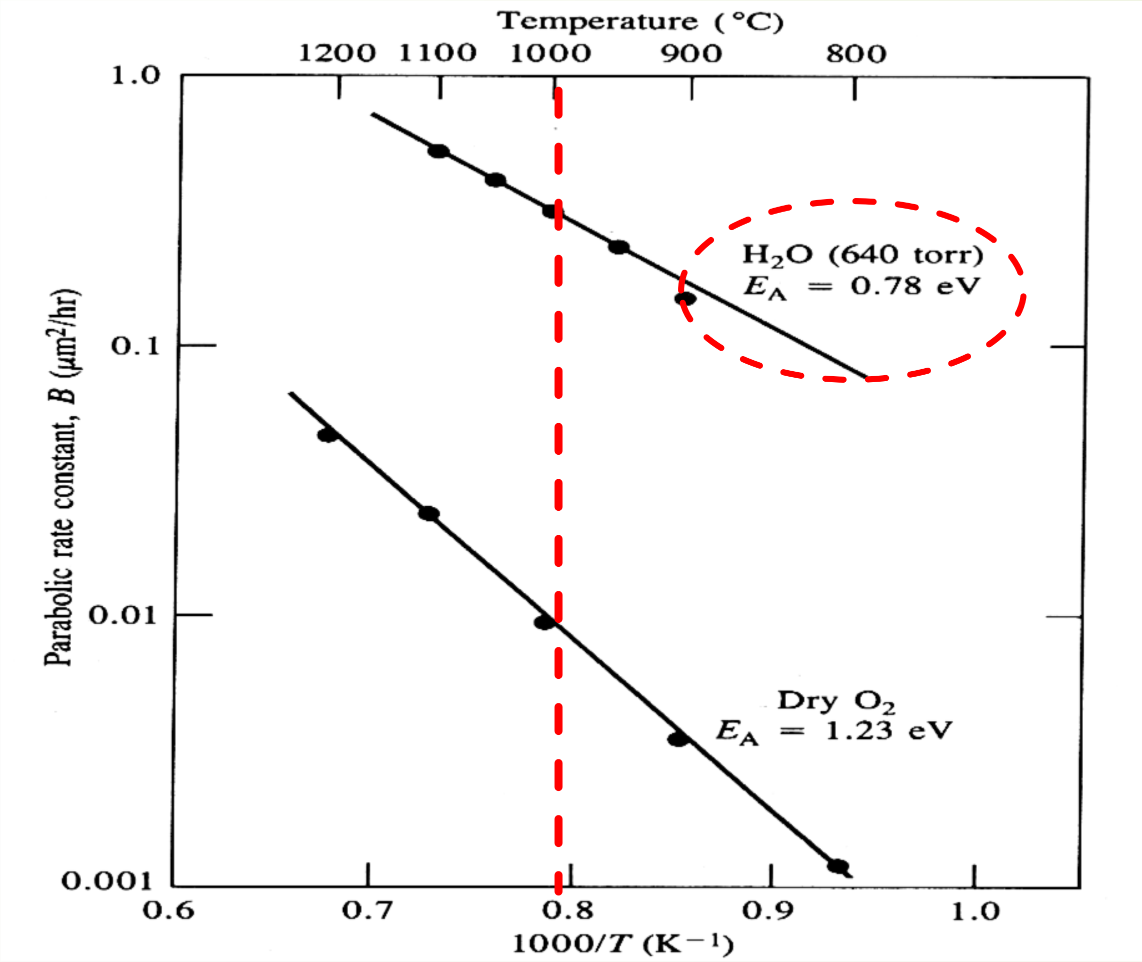
The energy required to break silicon-silicon bonds, 1.83 ev/molecule.

Factors Influencing Oxidation Rate

1. Temperature

✓ **For the same oxide thickness at a T → Time dry <<Time water vapor.**

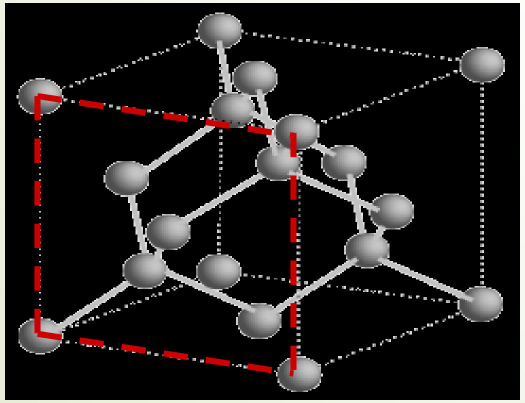




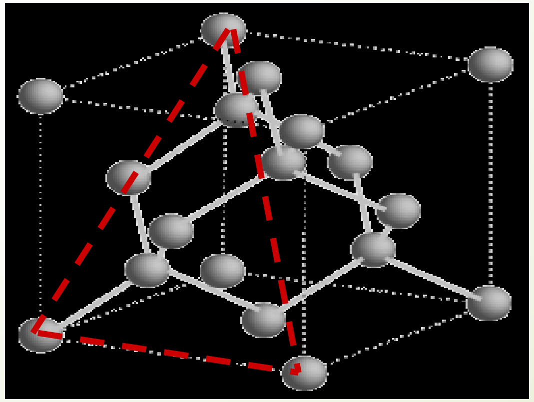
Factors Influencing Oxidation Rate

2. Wafer orientation

- The growth rate depends on the surface bond structure of silicon atoms.
- Large no of atoms allows faster oxide growth
- <111> plane have more Si atoms than <100> plane
  - Faster oxide growth in <111> Si



<100> plane



<111> plane

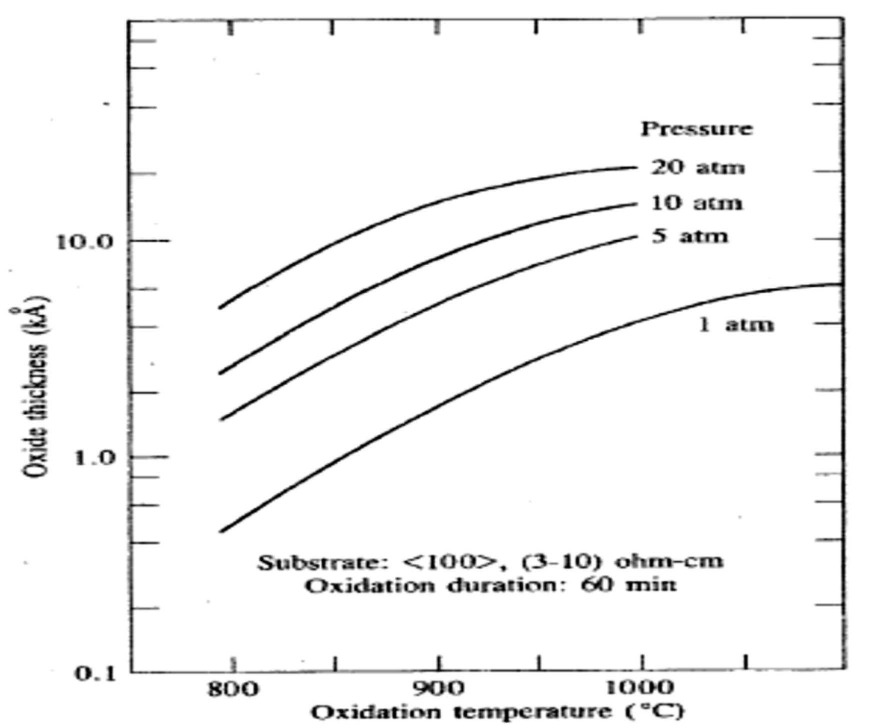
Factors Influencing Oxidation Rate

3. Pressure

- Pressure can be used to control oxide growth
- Both the linear (B/A) and parabolic rate (B) constants are proportional to $\boldsymbol{N_o}$.

$$A = \frac{2D}{K_s}, \qquad B = \frac{2DN_o}{M}$$

- N_o is proportional to the partial pressure of the oxidizing species
- High pressure is being used to increase oxidation rates for low temperatures
- Low-pressure oxidation control growth of thin oxides.



Factors Influencing Oxidation Rate

4. Wafer dopant(s) distribution

- Oxidized Si surface always has dopants; ***N-type*** or ***P-type*** from diffusion or ion implantation.
- During oxidation, the impurity concentration changes in the Si near the Si -SiO_2 interface.
- The impurity distribution depends on
  - a) **Dopant diffusion velocity**
  - b) **The oxide growing**
  - c) **Behavior of dopant**

Wafer dopant(s) distribution

a) Dopant diffusion velocity

- The impurity may diffuse rapidly through the silicon dioxide and escape to the gaseous ambient.

b) The oxide growing

- The relative rate of this oxide growth compared with the diffusion rate of the impurity through the oxide is important in determining the extent of the redistribution.

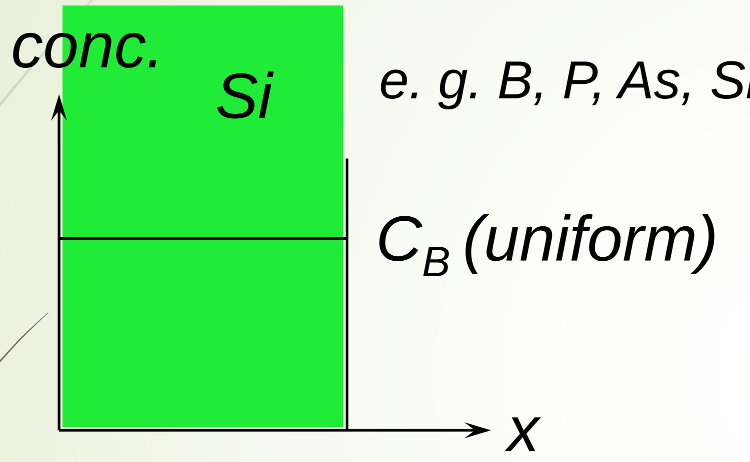
4. Wafer dopant(s) distribution

1. Behavior of dopant

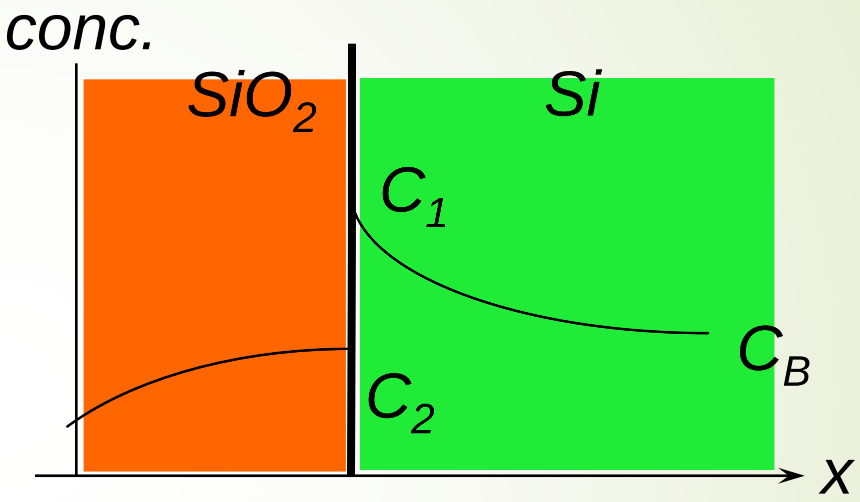
- When two solid are brought together, an impurity in one solid will redistribute between the two solids until it reaches equilibrium.
- ***Boron*** and ***gallium*** (N-type) tend to be depleted (يتقلص) from the surface; whereas ***phosphorus***, ***arsenic***, and ***antimony*** (P-type) pile up (يتراكم)at the surface. depend on both the *diffusion coefficient* and *the segregation coefficient* of the impurity in the oxide.
- *The segregation coefficient* ***m*** is

$$m = \frac{\text{Equilibrium concentration of impurity in silicon}}{\text{Equilibrium concentration of impurity in } SiO_2} \qquad (13)$$

1. Behavior of dopant



e. g. B, P, As, Sb.



Segregation Coefficient

$$m \equiv \frac{\textbf{equilibrium dopant conc. in Si}}{\textbf{equilibrium dopant conc. in } \mathbf{SiO_2}}$$

Fixed ratio

$$= \frac{C_1}{C_2}$$

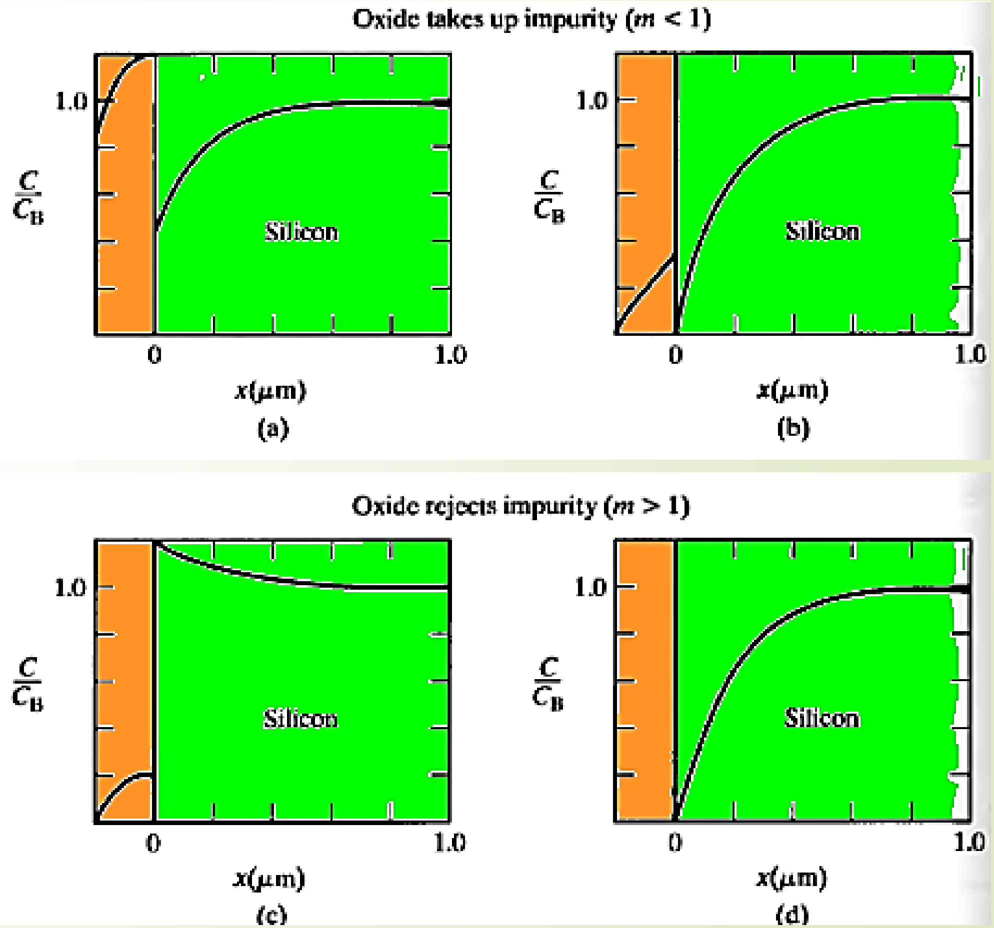
(can be>1 or <1)

4. Wafer dopant(s) distribution

- Four possible dopant redistribution processes are of interest:

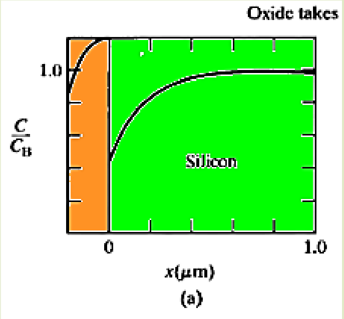
- ***In-group 1***, **m<1** the silicon surface is depleted of impurities;

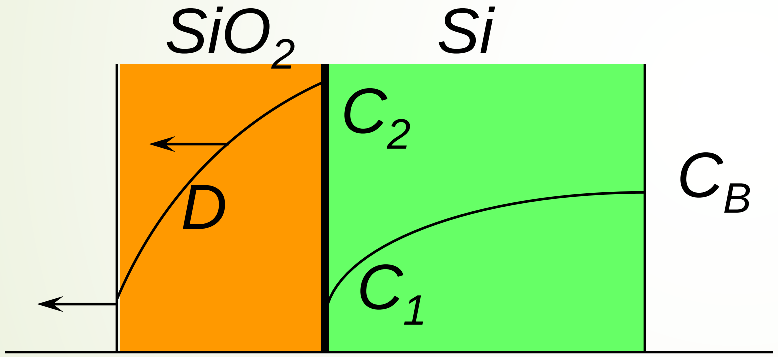
- ***In-group 2***, ***m* >1** the oxide piles up the impurity.



Four Cases of Interest (***In-group 1***, **m<1**)

(A) m < 1 and dopant diffuses slowly in SiO_2



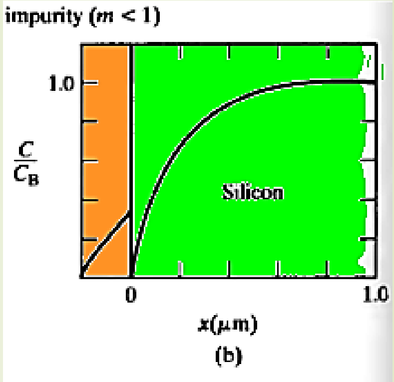


e. g. B (m = 0.3)

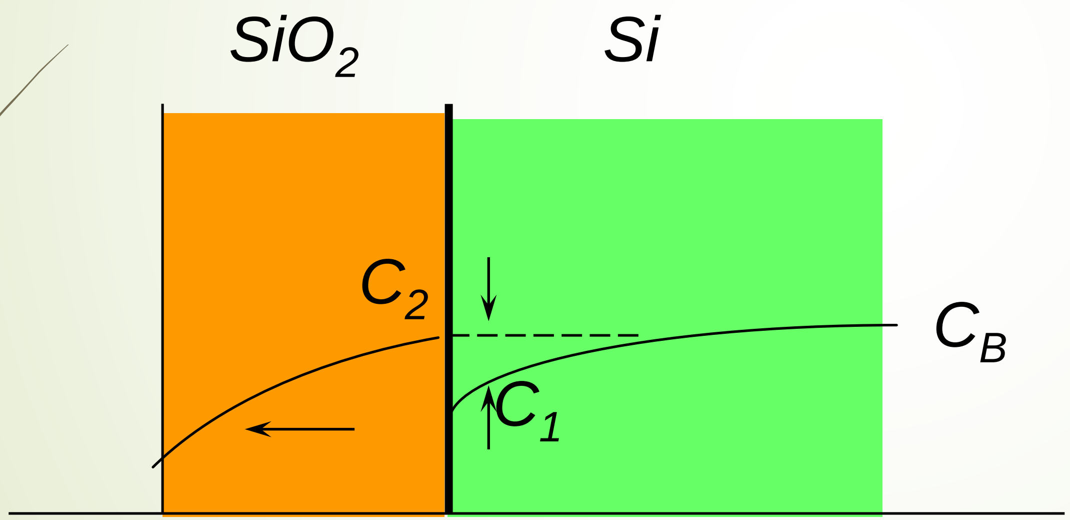
flux loss through SiO_2 surface not considered here.

$\Rightarrow$ B will be depleted near Si interface.

Four Cases of Interest (***In-group 1***, **m<1**)



(b) m < 1, dopant diffuses fast in SiO_2

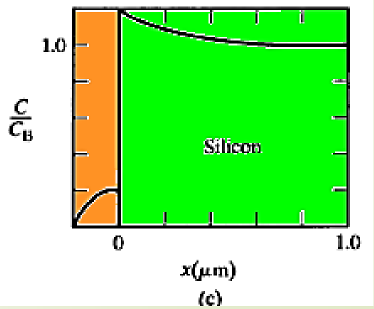


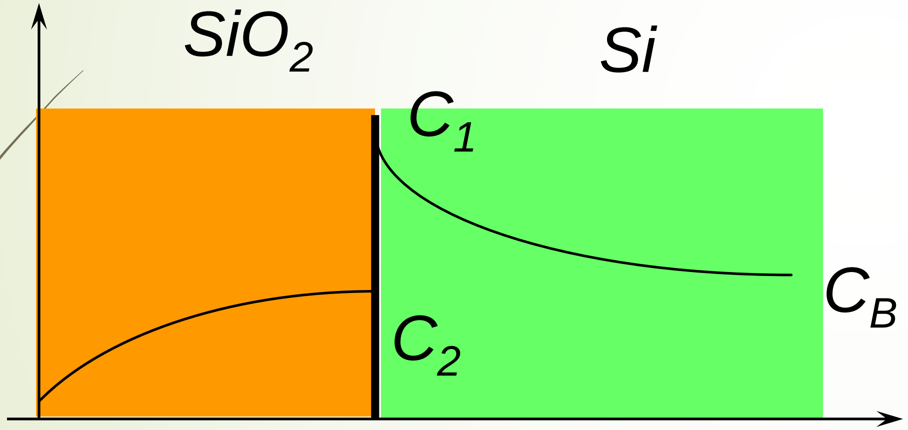
e. g. B, oxidize with presence of H_2

$\Rightarrow$ increases the amount of depletion

Four Cases of Interest (***In-group 2***, **m>1**)

(C) m > 1 and dopant diffuses slowly in SiO_2



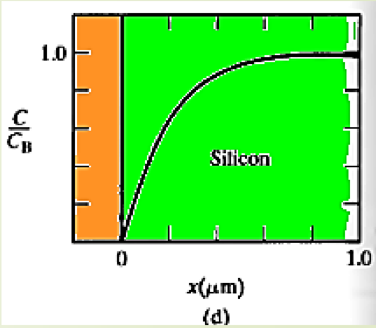


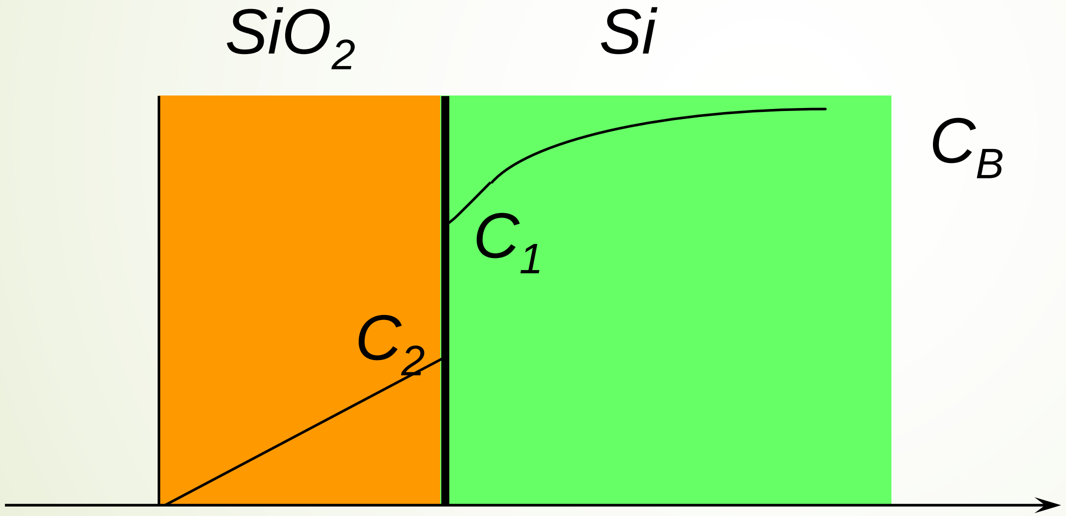
e.g. P, As, Sb

$\Rightarrow$ dopant piling up near Si interface for P, As & Sb

Four Cases of Interest (***In-group 2***, **m>1**)

(D) m > 1, dopant diffuses fast in SiO_2





e. g. Ga (m=20)

- Much impurity may escape from the solid to the gaseous ambient that the overall effect will be a depletion of the impurity;

Masking Properties Of Silicon Dioxide

- The most important properties of SiO_2 is its ability to mask impurities during high-temperature diffusion.

- The diffusivities of antimony, arsenic, boron, and phosphorus in SiO_2 << Si

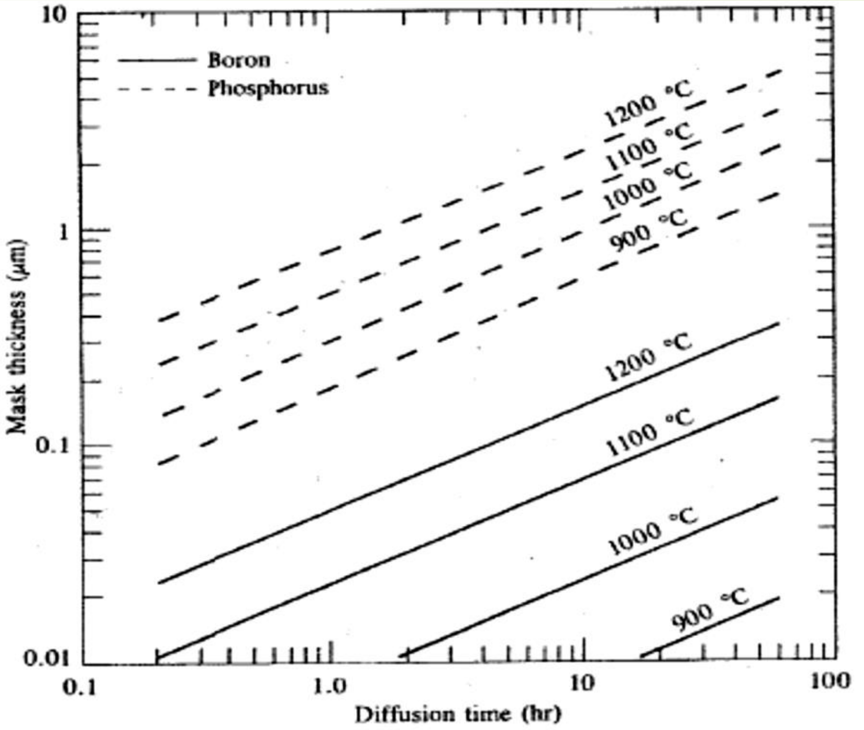


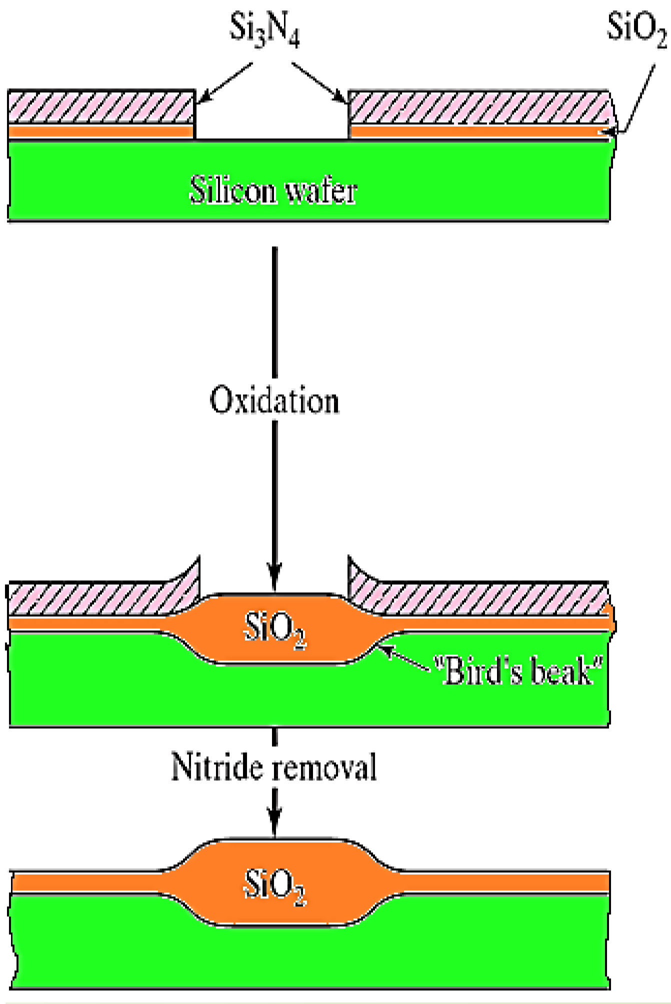
Fig. (11) Thickness of SiO_2 needed to mask boron and phosphorus diffusions as a function of diffusion time and temperature.

Selective Oxidation

- The oxidation processes generally form an oxide film over the complete surface of the silicon wafer.
- The ability to selectively oxidize result in improved device packing density and more planar final structures.
- Oxygen and water vapor do not diffuse well through silicon nitride.
- The selective oxidation process include
    1. *Semirecessed oxide structure*
    2. *Fully recessed oxide structure*

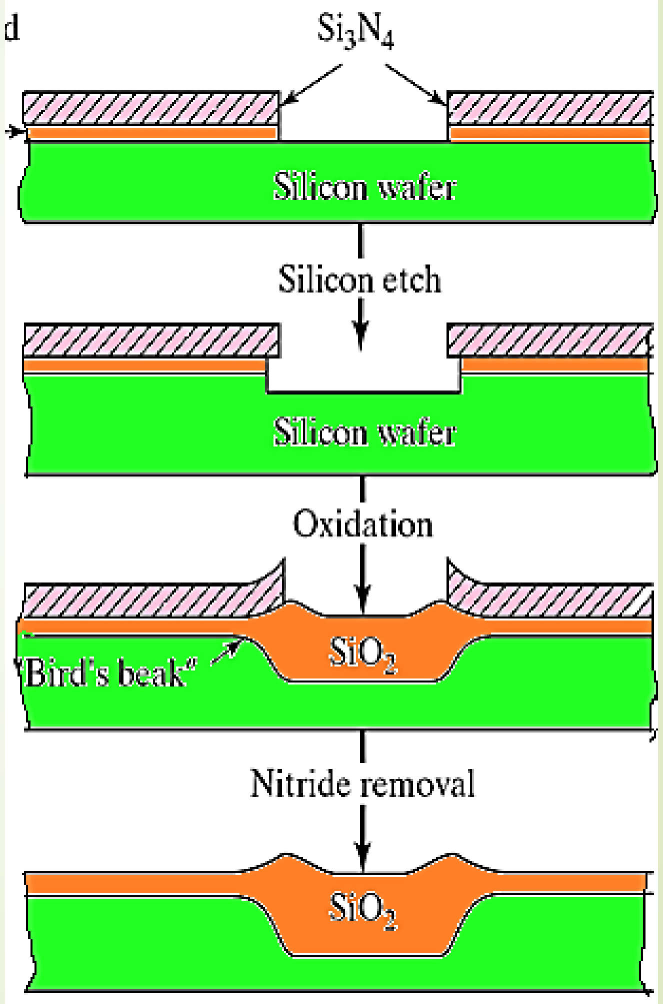
1. The *semirecessed* oxide structure

- A thin layer of SiO_2 is grown to protect the Si surface.
- A layer of silicon nitride Si_3N_4 is deposited over the SiO_2 surface patterned using photolithography.
- The thermal oxidation step is done.
- Some oxide growth occurs under the edges of the nitride and causes the nitride to bend up at the edges of the masked area "bird's beak"



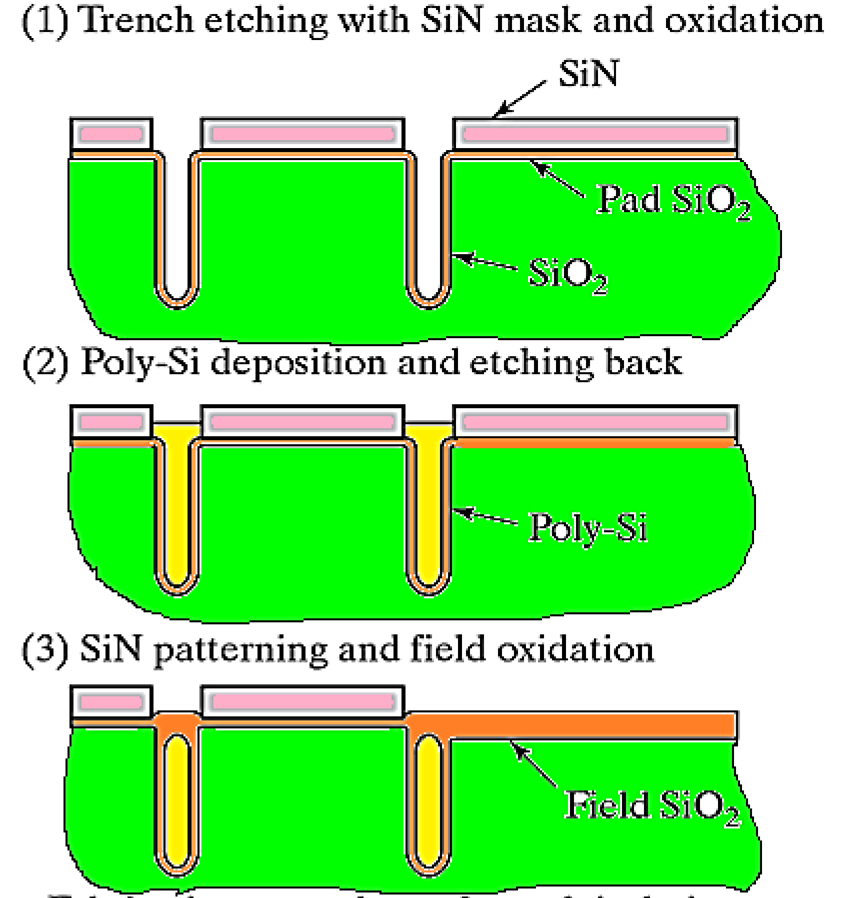
2. The *fully-recessed* oxide structure

- Etching the silicon prior to oxidation.
- Yield a very planar surface after the removal of the nitride mask.
- Provides isolation between nearby devices
- Minimize the bird's beak



Trench Formation

- ❑In most devices some shallow or deep refilled trench isolation is utilized.
- ❑ Often used in dynamic memory chips (DRAMS)
- ❑ Deep trenches used in high performance bipolar processes

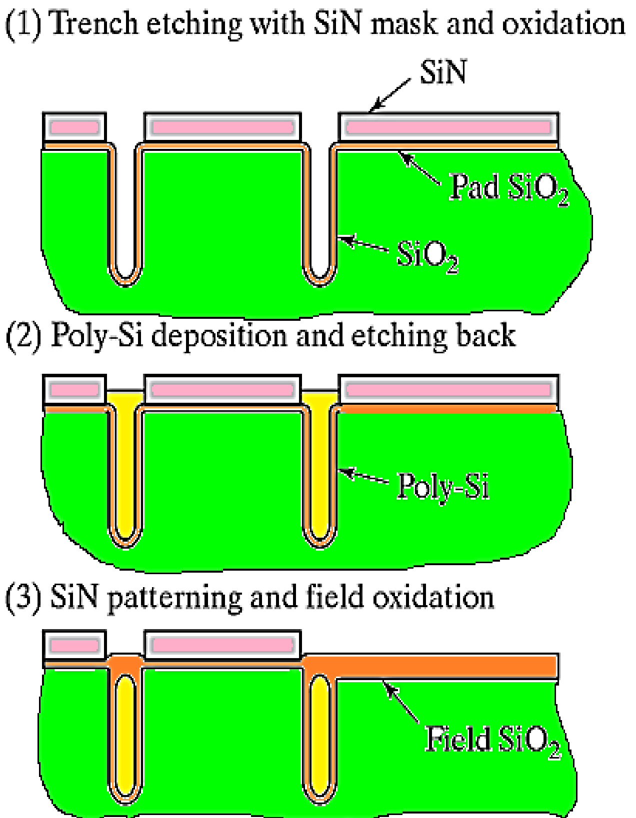


Fabrication procedure of trench isolation and field oxide.

(a) Deep-trench process

Trench Formation

- A thin SiO_2 pad is grown on Si
- A deposition of a silicon nitride SiN layer.
- Lithography is used to define openings in the nitride where trenches will be formed.
- The trenches are etched using reactive-ion etching
- The surface of the trench is passivated with a thin layer of thermally grown SiO_2
- The trench is refilled with deposited polysilicon.
- The final structure is produced by etching back any excess polysilicon, using a lithography .

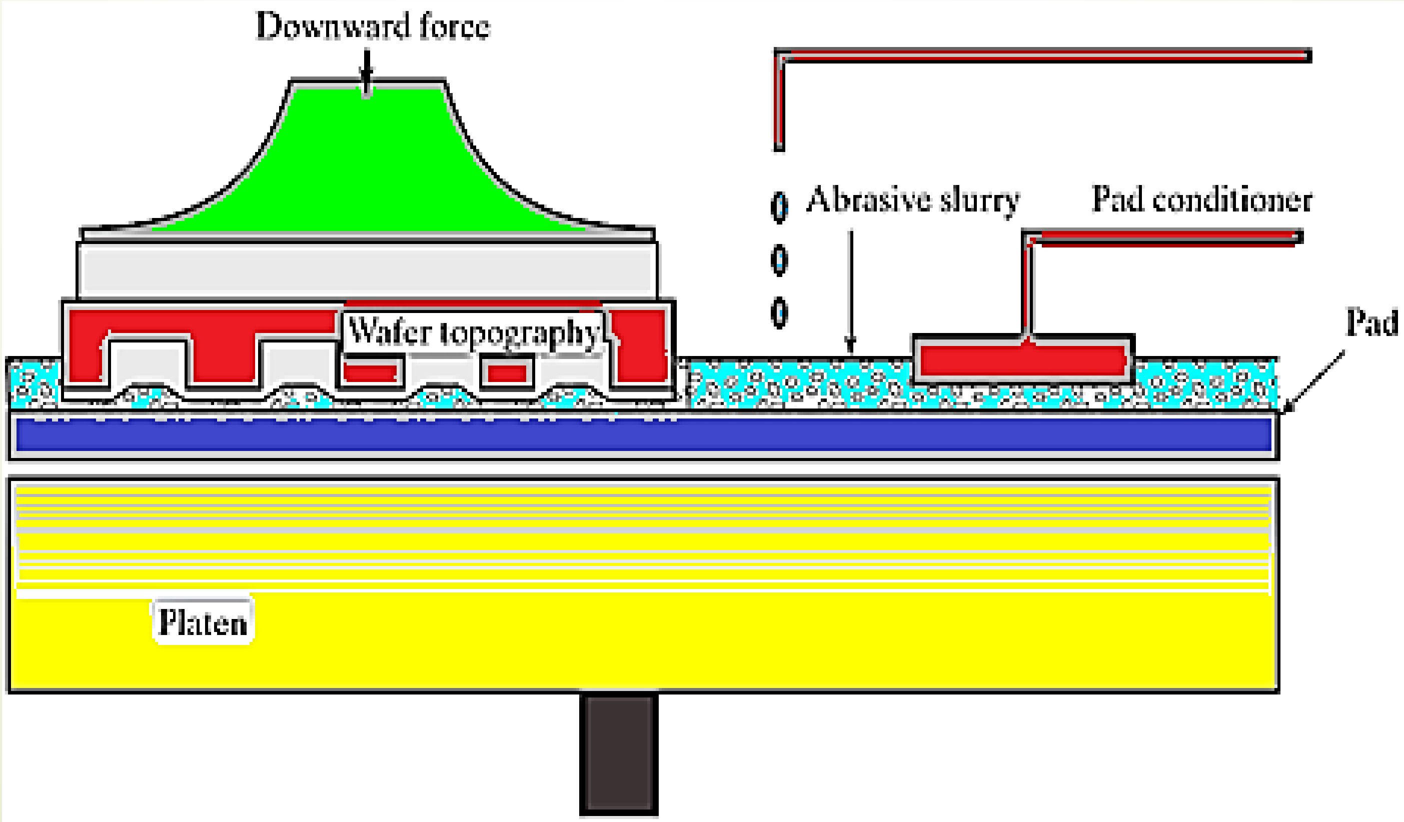


Fabrication procedure of trench isolation and field oxide.

(a) Deep-trench process

Chemical Mechanical Polishing (CMP)

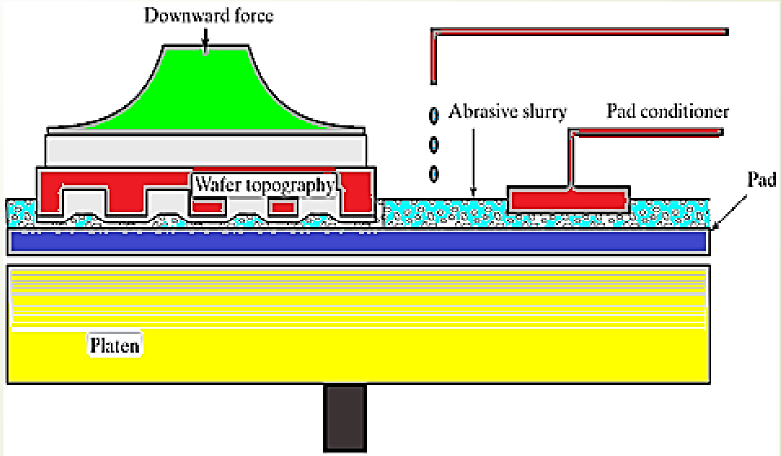
- ❑ Mechanical polishing is used to achieve highly planar surfaces
- ❑ Used in multilevel metallization systems including both aluminum and copper



Chemical Mechanical Polishing (CMP)

- The wafer is mounted on a carrier and is brought into contact with a polishing pad mounted on a rotating platen.
- A liquid slurry is continuously dispensed onto the surface of the polishing pad.

- A combination of the vertical force between the wafer and the abrasive pad as well as the chemical action of the slurry is used to polish the surface to a highly planar state.



Thank you

Q?

Discussion

- Why are oxides used as masks in device manufacturing?

Discussion

- **Why are oxides used as masks in device manufacturing?**

<u>Sol.</u>

1. Passivation of high-filed regions on the semiconductor surface.
2. Masking or prevention of diffusion except in selected areas.
3. Masking for selective doping (ion implantation).
4. As the insulation film in the gate region of MOS transistors.
5. Final circuit protection.

Discussion

- What is meant by the terms "wet oxide" and "dry oxide"?

Discussion

- **What is meant by the terms "wet oxide" and "dry oxide"?**

<u>Sol.</u>

- In a "dry" thermal oxide, the oxygen is supplied as pure O2 in gaseous form and the reaction is :

$$Si + O_2 \rightarrow SiO2$$

- If the oxygen is supplied in the form of steam "wet thermal oxide" the reaction is:

$$Si + 2H_2O \rightarrow SiO_2 + 2H2$$

Discussion

- What happens to donor and acceptor atoms in silicon during thermal oxidation?

Discussion

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Sol.

depend on both the *diffusion coefficient* and *the segregation coefficient* of the impurity in the oxide.

- ***Boron*** and ***gallium*** (N-type) tend to be depleted (يتقلص)from the surface; whereas
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Discussion

- When is Si_3N_4 sometimes used in place of an oxide?

Discussion

- **When is Si_3N_4 sometimes used in place of an oxide?**

Sol.

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- The ability to selectively oxidize result in improved device packing density and more planar final structures.
- The selective oxidation process include

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  2. Fully recessed oxide structure

Discussion

- If an oxide film is deposited at a rate of 70 nm/min, how long would it take to deposit 15000 Å?

Sol.

$$\text{Required Time} = t = \frac{Thickness}{Rate} = \frac{15000x10^{-10}}{70x10^{-9}} = 21.43 \text{ min}$$